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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/797,604	03/11/2004	Duk-min Yi	SEC.1066	3882
20987	7590 03/24/2005		EXAMINER	
	NE FRANCOS, & WH	QUINTO, KEVIN V		
	ONE FREEDOM SQUARE 11951 FREEDOM DRIVE SUITE 1260		ART UNIT	PAPER NUMBER
RESTON, V	'A 20190		2826	
			DATE MAILED: 03/24/2003	5

Please find below and/or attached an Office communication concerning this application or proceeding.

		Application No.	Applicant(s)	• •
Office Action Summary		10/797,604	YI ET AL.	
		Examiner	Art Unit	
		Kevin Quinto	2826	
Period f	The MAILING DATE of this communication app or Reply	oears on the cover sheet w	ith the correspondence address -	-
THE - Extended after - If the results of the result	MAILING DATE OF THIS COMMUNICATION. ensions of time may be available under the provisions of 37 CFR 1.1 or SIX (6) MONTHS from the mailing date of this communication. ee period for reply specified above is less than thirty (30) days, a reply operiod for reply is specified above, the maximum statutory period value to reply within the set or extended period for reply will, by statute or reply received by the Office later than three months after the mailing and patent term adjustment. See 37 CFR 1.704(b).	36(a). In no event, however, may a y within the statutory minimum of thi will apply and will expire SIX (6) MOI accuse the application to become A	reply be timely filed rty (30) days will be considered timely. NTHS from the mailing date of this communication BANDONED (35 U.S.C. § 133).	ation.
Status				
1)⊠ 2a)□ 3)□		s action is non-final. nce except for formal mat	• •	s is
Disposit	tion of Claims			
5)⊠ 6)⊠	Claim(s) <u>1-39</u> is/are pending in the application 4a) Of the above claim(s) is/are withdraw Claim(s) <u>1,2,19-26 and 34-39</u> is/are allowed. Claim(s) <u>3,11,27-33</u> is/are rejected. Claim(s) <u>4-10 and 12-18</u> is/are objected to. Claim(s) are subject to restriction and/o	wn from consideration.		
Applicat	tion Papers			
10)⊠	The specification is objected to by the Examine The drawing(s) filed on <u>11 March 2004</u> is/are: Applicant may not request that any objection to the Replacement drawing sheet(s) including the correct The oath or declaration is objected to by the Ex	a) accepted or b) dob drawing(s) be held in abeya tion is required if the drawing	nce. See 37 CFR 1.85(a). g(s) is objected to. See 37 CFR 1.12	• •
Priority	under 35 U.S.C. § 119			
12)[a)	Acknowledgment is made of a claim for foreign All b) Some * c) None of: 1. Certified copies of the priority document 2. Certified copies of the priority document 3. Copies of the certified copies of the priority document application from the International Bureau See the attached detailed Office action for a list	s have been received. s have been received in A rity documents have beer u (PCT Rule 17.2(a)).	Application No received in this National Stage	
Attachmer	• •	ο 🗆	(DTO 440)	
2)	ce of References Cited (PTO-892) ce of Draftsperson's Patent Drawing Review (PTO-948) rmation Disclosure Statement(s) (PTO-1449 or PTO/SB/08) er No(s)/Mail Date	Paper No(Summary (PTO-413) s)/Mail Date nformal Patent Application (PTO-152) 	

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DETAILED ACTION

Drawings

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: 761c in figure 7(a), all reference numbers in figure 7(b), a line without a reference number in figure 8(a). Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

- The following is a quotation of the second paragraph of 35 U.S.C. 112:
 The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.
- 3. Claims 27-33 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

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4. Claim 27 recites the limitation "said array of source/drain regions" in line 20, p.31 of the disclosure filed March 11, 2004. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

- (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
- 6. Claims 3 and 11 are rejected under 35 U.S.C. 102(b) as being anticipated by Hsing et al. (USPN 5,517,046).
- 7. In reference to claim 3, Hsing et al. (USPN 5,517,046, hereinafter referred to as the "Hsing" reference) discloses a similar device. Figures 4 and 5 each illustrate a device which meets the limitation of claim 3. Figure 6 illustrates a plan view which applies to both figures 4 and 5. Figures 4 and 5 of Hsing each illustrate a semiconductor device with a mesh-shaped gate electrode (26) located over a surface of a substrate (20). The mesh-shaped gate electrode (26) has a plurality of openings aligned over respective source/drain regions (32, 34) of the substrate (20). A gate dielectric layer (24) is interposed between the mesh-shaped gate electrode (26) and the surface of the substrate (20). At least one oxide region (33) is located in the substrate (20) below the mesh-shaped gate electrode (26). A thickness of the oxide region (33) is greater than that of the gate dielectric (24).

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- 8. With regard to claim 11, the oxide region (33) is a field oxide region.
- 9. Claims 27, 28, 32, and 33 are rejected under 35 U.S.C. 102(b) as being anticipated by Hsing et al. (USPN 5,517,046).
- 10. So far as understood in claim 27, Hsing (USPN 5,517,046) discloses a similar device. Figures 4 and 5 each illustrate a device which meets the limitation of claim 19. Hsing makes it clear that figure 8 is nearly identical buy also illustrates a plan view which applies to both figures 4 and 5 (column 6, lines 51-55). Figures 4 and 5 of Hsing each illustrate a semiconductor device with a mesh-shaped gate electrode (26) located over a surface of a substrate (20). The mesh-shaped gate electrode (26) has a plurality of openings aligned over respective source/drain regions (32, 34) of the substrate (20. A gate dielectric layer (24) is interposed between the mesh-shaped gate electrode (26) and the surface of the substrate (20). At least one oxide region (33) is located in the substrate (20) below the mesh-shaped gate electrode (26). A thickness of the oxide region (33) is greater than that of the gate dielectric (24). Figure 7 shows another cross-section of the device. A dielectric layer (47) is formed over the semiconductor substrate (20) and the mesh-shaped gate electrode (26). There is a plurality of elongate drain electrodes (54) which are located over the dielectric layer (47) and extend parallel to each other and diagonally over the source/drain regions (32, 34). There is a plurality of elongate source electrodes (52) which are located over the dielectric layer (47) and extend parallel to each other and diagonally over the source/drain regions (32, 34). The source electrodes (52) and the drain electrodes (54) are alternately arranged over the dielectric layer (47).

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11. With regard to claim 28, the oxide region (33) comprises an array of oxide regions located below the gate intersection regions of the mesh-shaped gate electrode.

- 12. In reference to claim 32, the elongate source electrodes (52) and the elongate drain electrodes (54) are coplanar.
- 13. With regard to claim 33, the oxide region (33) is a field oxide region.

Allowable Subject Matter

- 14. Claims 1, 2, 19-26, and 34-39 are allowed.
- 15. Claims 4-10 and 12-18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.
- 16. The following is a statement of reasons for the indication of allowable subject matter: the examiner is unaware of any prior art which suggests or renders obvious a field effect transistor using a mesh type gate, a mesh type electrode for the source or drain formed over a first dielectric layer and another mesh type electrode for the source or drain formed over a second different dielectric layer.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin Quinto whose telephone number is (571) 272-1920. The examiner can normally be reached on M-F 8AM-5PM.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KVQ

NATHAN J. FLYNN SUPERVISORY PATENT EXAMINER

TECHNOLOGY CENTER